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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,784	782,784 02/23/2004		Jong-Hyuk Baek	P-0646	5504
34610	7590	12/29/2005		EXAMINER	
FLESHNER		LLP	COX, CASSANDRA F		
P.O. BOX 22 CHANTILL		0153		ART UNIT	PAPER NUMBER
				2816	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/782,784	BAEK, JONG-HYUK				
Office Action Summary	Examiner	Art Unit				
	Cassandra Cox	2816				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply is specified above, the maximum statutory period was Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	i6(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days ill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONEI	nely filed s will be considered timely. the mailing date of this communication. O (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on 14 Oc	ctober 2005.					
	action is non-final.					
3) Since this application is in condition for allowan						
Disposition of Claims						
4) ☐ Claim(s) 1-9,11-15 and 18-20 is/are pending in 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-9,11-15 and 18-20 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or	vn from consideration.					
Application Papers						
9) The specification is objected to by the Examiner 10) The drawing(s) filed on 23 February 2004 is/are Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction 11) The oath or declaration is objected to by the Examiner	: a)⊠ accepted or b)⊡ objected drawing(s) be held in abeyance. See on is required if the drawing(s) is obj	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
a) All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list of	s have been received. s have been received in Application ity documents have been received (PCT Rule 17.2(a)).	on No ed in this National Stage				
Attachment(s)	_					
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/14/05.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	(PTO-413) ite atent Application (PTO-152)				

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DETAILED ACTION

1. Applicant's arguments with respect to claims 1-9, 11-15, and 18-20 have been considered but are most in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 3. Claims 1-2, 4, 6, 8-9, 11, 14-15, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Lind (U.S. Patent No. 4,704,585).

In reference to claim 1, Lind discloses in Figure 4 a phase lock loop circuit comprising: a memory (114) to store control voltages; and a processor (110) to load a control voltage, which corresponds to a changed channel (from channel selector 112), from the memory (114) when a system channel is changed, and to provide the control voltage to a Voltage Control Oscillator (102), see ABSTRACT. The same applies to claims 2, 4, 8-9, 11, 15, and 19, wherein the method includes the step of setting the control voltage as an initial control voltage (since it is the only source of the control voltage it is also seen to supply the initial control voltage).

In reference to claim 6, Lind discloses in Figure 4 the PLL circuit further including a signal converter (106) to convert control voltage information to an analog signal and transmit the analog signal to the VCO (102). The same applies to claim 14.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

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granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-9, 11-15, 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Camp, Jr. (U.S. Patent No. 6,380,809).

In reference to claim 1, Camp discloses in Figure 2 a phase lock loop circuit comprising: a memory (105) to store control voltages; and a processor (90) to load a control voltage, which corresponds to a changed channel, from the memory (105) when a system channel is changed, and to provide the control voltage to a Voltage Control Oscillator (95). The same applies to claims 4, 8-9, 11, 15, and 19, wherein the method includes the step of setting the control voltage as an initial control voltage (the first channel request from PLL 60 is used as the initial control voltage).

In reference to claim 3, Camp discloses Figure 2 that once the control voltage of the memory (105) is provided to the VCO (95), the processor (90) cuts off a path between the memory (105) and the VCO (95), this is done by controlling switch 70 to again receive a channel request from PLL 60. The same applies to claim 7, wherein the signal converter is disabled by the reconnection of switch 70 to the PLL (60).

In reference to claim 5, Camp discloses in Figure 2 the PLL circuit further including a signal converter (100) to convert a control voltage to a digital signal and transmit the digital signal to the memory (105). The same applies to claims 6, 12, 14, and 18, wherein circuit also comprises a signal converter (80) to convert control voltage information of the memory to an analog signal and transmits the analog signal to the VCO (95).

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In reference to claim 13, Camp discloses in Figure 3 wherein storing the control voltages includes repeating the obtaining, the converting and the storing until control voltages for every channel of a system are obtained (this is done by repeating the process for every channel request received from PLL 60).

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Camp, Jr. (U.S. Patent No. 6,380,809).

Camp discloses all the limitations of the claim as mentioned above with respect to claim 15. In addition, Camp discloses in Figure 1 a frequency generator (34), a phase detector (28), a loop filter (30), and a first frequency divider (36). Camp does not disclose a second frequency divider. However, phase locked loops including additional frequency dividers are well known in the art. It would have been obvious to one skilled in the art at the time of the invention that a second frequency divider could be added to the phase locked loop (26) of Camp for the advantage of providing additional frequency shifted output clocks that can be used in other systems needing clocks of different frequencies than the standard output clock of the PLL.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

December 17, 2005

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800